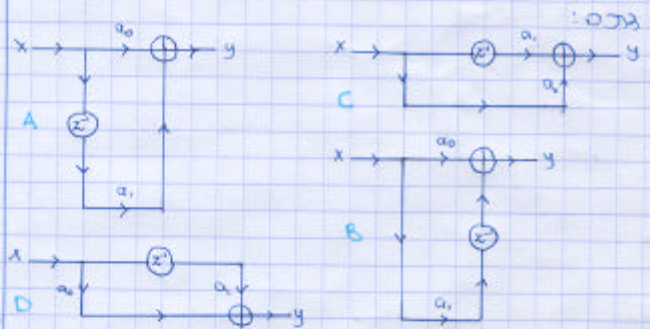




$y_n = a_0 x_n + a_1 x_{n-1}$



התבונה של המודל הזה



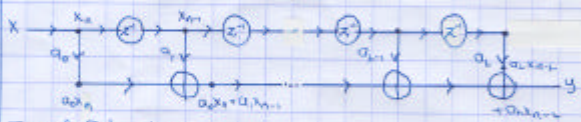
התבונה של המודל הזה

$y_n = \sum_{k=0}^L a_k x_{n-k}$

MA x CF



התבונה של המודל הזה



התבונה של המודל הזה

Tapped Delay Line

התבונה של המודל הזה

Multiply-And-Accumulate (MAC)

$u \rightarrow u \cdot a \cdot b$



התבונה של המודל הזה

התבונה של המודל הזה

התבונה של המודל הזה

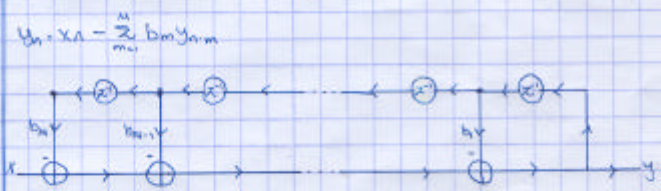
2

Feedforward network structure, or even all over the way to now feedback network

$y_n = x_n + b_1 y_{n-1}$



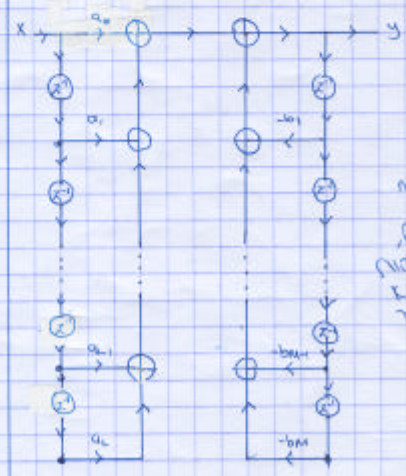
$y_n = x_n + \sum_{m=1}^M b_m y_{n-m}$



(AR) All-pole network  
MTC filter structure

Good for noise reduction

$y_n = \sum_{k=0}^L a_k x_{n-k} - \sum_{m=1}^M b_m y_{n-m}$



ARMA

ARMA structure is a combination of AR and MA. AR is all-pole and MA is zero-pole. ARMA is a combination of both. It is used for modeling systems with both poles and zeros. The feedback part (AR) helps in noise reduction and the feedforward part (MA) helps in shaping the frequency response.





מבנה מחשב 18.2

המחשב מורכב מ- CPU, Memory, I/O, Bus, ALU, Register, PC, Instruction Memory, Data Memory, Cache, Main Memory, Disk, Network, etc.  
 (2) load x → x || load y → y

fetch, decode, execute, memory access, write back  
 (1) update pointer to x || update pointer to y  
 (3) load x to register x || load y to register y  
 (5) MAC:  $a \leftarrow a + x$

Pipeline 18.3

update 1	update 2	update 3	update 4	update 5		
	load 1	load 2	load 3	load 4	load 5	
		MAC 1	MAC 2	MAC 3	MAC 4	MAC 5

pipeline of a MAC  
 5-stage pipeline  
 T = N + D - 1

(fetch, decode, execute) 3

Interrupts, Ports 18.4

context switch  
 interrupt  
 Interrupt Service Routine  
 zero-overhead b. def - a

ports

serial in  
 serial out  
 Direct Memory Access (DMA)  
 bus

fixed and floating point 18.5

fixed point  
 floating point  
 overflow  
 optional scaling generator  
 pipeline

FFT 18.6

FFT  
 butterfly  
 $N = 2^m$   
 $A = T$   
 $A = T$















